CLAIMS:

1. (Currently amended) A data writing/reading method of sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction; wherein when plural data having written into the memory at present are read in a row direction, plural data which is the next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

2. (Cancelled)

3. (Previously presented) A data writing/reading method as claimed in claim 1, wherein plural data are arranged into the memory in matrix structures having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.

4. (Currently amended) A method of de-interleaving by sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the

first read direction; wherein when plural data having written into the memory at present are read in a row direction, plural data which is the next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

5. (Cancelled)

6. (Previously presented) A de-interleaving method as claimed in claim 4, wherein interleaved plural data are arranged into the memory in matrix structures having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.

7. (Currently amended) A data processing method comprising a first step of interleaving a plurality of data, and a second step of de-interleaving by sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction; wherein the second step is characterized in that when plural data having written into the memory at present are read in a row direction, plural data which is the next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

8. (Cancelled)

9. (Previously presented) A data processing method as claimed in claim 7, wherein the first step contains configuring a super frame having plural frames, each of the frames formed by arranging plural data in matrix form, and contains interleaving the plural data configuring the super frame.

10. (Previously presented) A data processing method as claimed in claim 7, wherein the second step is characterize in that interleaved plural data are arranged into the memory in matrix structures having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.

11. (Previously presented) A data processing method as claimed in claim 10, wherein the first step is characterized by configuring a super frame having eight frames, each of the frames formed by arranging (203x48) data in matrix form, and is characterized by interleaving (203x48x8) data configuring the super frame, and the second step is characterized in that when (203x48x8) data having written into the memory at present are read in a row direction, (203x48x8) data which is the next to be written are sequentially written in the row direction, on the other hand, when (203x48x8) data having written into the memory at present are read in a column direction, (203x48x8) data which is the next to be written are sequentially written in the column direction.

12. (Previously presented) A data processing method as claimed in claim 11, wherein the second step is for arranging (203x48x8) data into the memory in 48 matrix structures, each of the 48 matrix structures formed from (203x8) data, and each of the 48 matrix structures is the structure having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.

13. (Previously presented) A data processing method as claimed in claim 12, wherein each of the 48 matrix structures is the structure having 8 by 8 blocks, each of the blocks having 26 addresses, and each of the blocks for writing one

data into an area corresponding to the one address of each of the blocks, and the second step is for writing one data into the area corresponding to the one address of each of the blocks.

14. (Previously presented) A data processing method as claimed in claim 12, wherein each of the 48 matrix structures is the structure having 8 by 8 blocks, each of the blocks having 4 addresses, and each of the blocks for writing 7 data into an area corresponding to the one address of each of the blocks, and the second step is for writing the 7 data into the area corresponding to the one address of the matrix structures.

15. (Currently amended) A memory for sequentially writing a plurality of data in a write direction and sequentially reading the written data in a read direction characterized in that a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction; wherein when plural data having written into the memory at present are read in a row direction, plural data which is the next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

16. (Currently amended) A memory drive apparatus for sequentially writing a plurality of data in a write direction and sequentially reading the written data in a read direction characterized in that a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction; wherein when

plural data having written into the memory at present are read in a row direction, plural data which is the next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

17. (Cancelled)

18. (Previously presented) A memory drive apparatus as claimed in claim 17, wherein the apparatus provides with addressing means for addressing the memory, and by sequentially addressing the memory with the addressing means, plural data are arranged into the memory in matrix structures having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.